

# 185 GHz Monolithic Amplifier in InGaAs/InAlAs Transferred-Substrate HBT Technology

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**Abstract** — We report a single-stage tuned amplifier that exhibits a peak small signal gain of 3.0 dB at 185 GHz. To the best of our knowledge, this is the first reported HBT result for a tuned amplifier at this frequency, and the gain-per-stage compares favorably with results from HEMT technologies. The amplifier was designed in a transferred-substrate HBT technology that has exhibited record values of extrapolated  $f_{max}$  ( $>1$  THz).

## I. INTRODUCTION

Electronics in the 140-220 GHz frequency range have applications in remote atmospheric sensing, wideband communication systems, and automotive radar. Monolithic amplifiers in this frequency range have previously been demonstrated in InGaAs/InAlAs HEMT technologies with electron beam written gate fingers [1]-[3]. Multi-stage amplifiers in these technologies have exhibited large small signal gains. Weinreb et al [1] have reported a six-stage amplifier providing  $20 \pm 6$  dB gain from 150 to 215 GHz, and Pobanz et al [2] have demonstrated an eight-stage amplifier with  $17 \pm 2$  dB gain from 150 to 205 GHz.

InGaAs/InAlAs transferred-substrate HBTs have demonstrated record RF figures of merit,  $f_t > 295$  GHz and  $f_{max} > 1$  THz [4,5], when emitter and collectors are scaled to sub-micron dimensions. Previous amplifiers designed in this technology have included: an 80 GHz traveling-wave amplifier with 11.5 dB mid-band gain [6], a Darlington resistive feedback amplifier with 15.6 dB gain and  $> 50$  GHz bandwidth [7], and tuned W-band power amplifiers delivering 10 dBm at 78 GHz [8]. Larger ICs include 66 GHz master-slave flip flops [9] and 18 GHz delta-sigma ADCs [10]. Here, we report a single stage tuned amplifier that exhibits 3.0 dB peak gain at 185 GHz. While the gain is substantially lower than those reported for multi-stage HEMT amplifiers, it is comparable to the gain-per-stage reported for the circuits. Also, we believe this to be the first HBT tuned amplifier reported in this band.

## II. TRANSFERRED-SUBSTRATE HBT TECHNOLOGY

The following section provides a brief overview of the transferred-substrate HBT process. The substrate transfer process provides access to both sides of the device epitaxial material, which allows for the simultaneous definition of narrow emitter and collector stripes. The collector-base capacitance ( $C_{cb}$ ) is determined by the area of the collector contact, and not by the area of the base mesa, as in a traditional mesa HBT. High values of transistor power-gain cutoff frequency ( $f_{max}$ ) can be obtained by aggressively scaling the emitter and collector stripe dimensions. In this work, electron beam lithography was used to define submicron emitter and collector stripes.

### A. Growth and Fabrication

The MBE epitaxial structure is grown on a Fe-doped semi-insulating InP substrate. The HBT has a single InAlAs/InGaAs heterojunction. A Schottky collector contact eliminates the need for a sub-collector layer and eliminates extrinsic collector resistance. The InGaAs collector thickness used in this work was 300 nm. To reduce collector transit time and increase  $f_t$ , transistors have been fabricated with collectors as thin as 150 nm. The thicker collector results in a very large  $f_{max}$  to  $f_t$  ratio ( $\approx 4:1$ ), but this is acceptable for tuned circuit applications. The 40 nm base layer is p+ Be doped at  $5 \times 10^{19}$  cm<sup>-3</sup>, and includes approximately 50 mV of compositional grading to reduce base transit time.

Fig. 1 shows a schematic cross-section of the transferred substrate HBT. The fabrication begins with the evaporation of Ti/Pt/Au emitter contacts. The electron beam lithography system at UCSB has been used to realize emitter widths as narrow as 0.2  $\mu$ m. A base contact etch is followed by the deposition of self-aligned base metal. Isolation mesas are then etched and a polyimide passivation layer is spun on the wafer. The polyimide is etched back to expose the emitter fingers.

Thin-film NiCr resistors are deposited with a sheet resistance of  $50\Omega/\text{square}$ . The first metal interconnect layer (M1) is then deposited. This layer forms a majority of the transmission lines and interconnects, and provides contact to the emitter and base metals. The metal also serves as the bottom plate for MIM capacitors, which are formed by a blanket deposition of SiN over the entire wafer. The SiN is etched away where contact between M1 and the second metallization (M2) layer is required. The M2 layer also forms the top plate for the MIM capacitors.

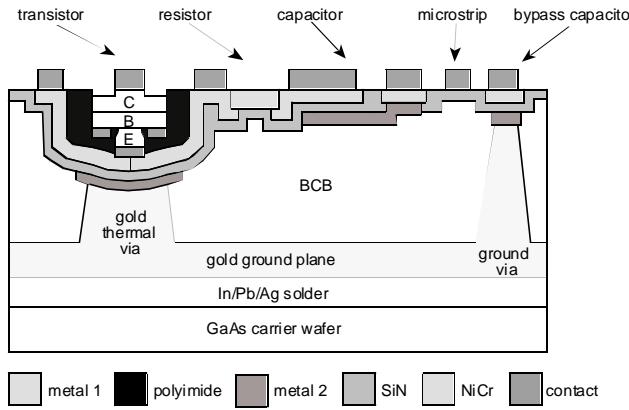


Fig. 1. Schematic cross-section of transferred-substrate HBT process.

Benzocyclobutene ( $\epsilon_r=2.7$ ) is spun onto the wafer and serves as the microstrip dielectric. Vias are dry-etched in the BCB to M2, and the BCB is simultaneously etched back to a final thickness of  $5\mu\text{m}$  relative to the bottom of the M1 transmission lines. The vias are used for electrical grounding, and to provide heat sinking for the devices. Gold plating is then performed to fill vias and form a continuous ground plane.

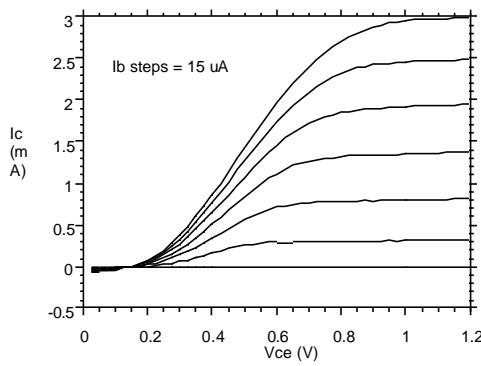


Fig. 2. DC common-emitter characteristics of submicron transferred substrate HBT ( $0.4\mu\text{m} \times 0.6\mu\text{m}$  emitter junction area).

The wafer is then solder bonded to a GaAs carrier wafer of similar size and shape. An HCl etch removes the entire InP substrate and exposes the collector semiconductor. The collector stripes were also defined with e-beam lithography. Local alignment marks are used for each individual transistor during the collector write. This is necessary for narrow collector devices due to a  $3 \times 10^{-4}$  fractional shrinkage that is observed after substrate transfer. Transistors with collectors as narrow as  $0.3\mu\text{m}$  have been realized. After collector deposition, a self-aligned wet etch of  $\approx 50\text{ nm}$  depth removes the collector junction side walls. This etch is intended to eliminate fringing fields and decrease  $C_{cb}$ . For devices with sub-micron collectors, in particular, the resulting increase in  $f_{max}$  is greater than one would predict from the reduction in  $C_{cb}$ .

### B. Device Results

Common-emitter DC characteristics of a submicron transferred substrate HBT are shown in Fig. 2. The device has an emitter junction area of  $0.4\mu\text{m} \times 6\mu\text{m}$ , and a collector stripe of  $0.7\mu\text{m} \times 9\mu\text{m}$ . The device has a DC small signal current gain,  $b$ , of 20. The device has a common-emitter breakdown voltage  $BV_{CEO}$  of 1.5 V at a current density of  $10^5\text{ A/cm}^2$ .

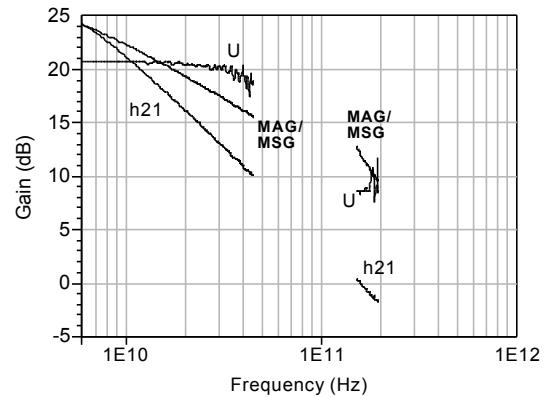


Fig. 3. HBT current gain ( $h_{21}$ ), maximum stable power gain (MSG) and unilateral power gain (U), measured in the DC-45 GHz and 140-200 GHz bands.

The devices were characterized by on-wafer network analysis from 1 to 45 GHz and from 140 to 220 GHz. Fig. 3 shows the maximum available/stable gain MAG/MSG, the short-circuit current gain  $h_{21}$ , and Mason's invariant (unilateral) power gain U of a transistor with the device dimensions previously specified. Measurement calibration was performed using on wafer Thru-Reflect-Line (TRL) calibration standards.

The measured  $f_t$  of the device was 160 GHz. Accurately predicting the value of  $f_{max}$  from measurements is difficult because of the sensitivity of  $U$  to measurement inaccuracies in the 140 to 220 GHz band. However, measurements do indicate the devices fabricated in this particular process run have poorer RF characteristics than previously realized submicron HBTs [4].

### III. AMPLIFIER DESIGN

The amplifier design was based on a hybrid-pi transistor model developed from an earlier generation e-beam lithography device [4]. The model was developed from on-wafer S-parameter measurements from 1 to 50 and 75 to 110 GHz. The device used in the design had an emitter junction area of  $0.4 \mu\text{m} \times 6 \mu\text{m}$ , and a collector stripe of  $0.7 \mu\text{m} \times 9 \mu\text{m}$ .

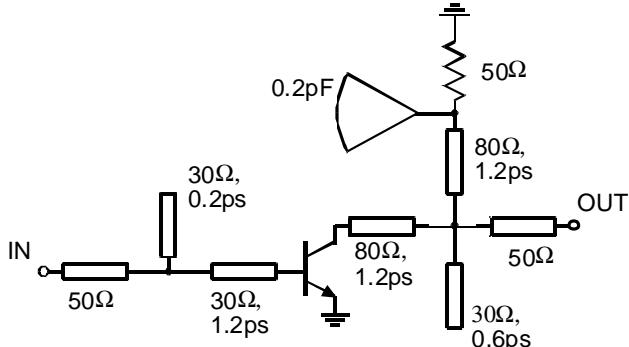


Fig. 4. Schematic diagram of single stage amplifier design.

Fig. 4 shows the schematic diagram for the amplifier. A simple common emitter configuration was used with shunt stub tuning at the input and output. A shunt resistor at the output was used to ensure low frequency stability, and a quarter-wave line to a radial stub capacitor bypassed the resistor at the design frequency. DC bias T's built into the on-wafer probes allowed bias to be applied at the input and output of the amplifier. The intended design frequency for the amplifier was 200 GHz, and in simulations the amplifier was conjugately matched at this frequency. Fig. 5 shows a photograph of the fabricated amplifier.

Due to the high design frequency, electromagnetic simulation of passive elements was performed. Agilent's Momentum EM simulator was used to model the resistor/radial stub network and any microstrip discontinuities in the circuit. EM simulations also showed that the SiN ( $\epsilon_r = 7$ ) that is blanket deposited over the wafer before BCB deposition changes the effective dielectric constant of the microstrip

transmission lines by approximately 20%. In the final design, the SiN was etched away around the transmission lines so that standard microstrip CAD models could be used.

The 5  $\mu\text{m}$  BCB microstrip dielectric used in the transferred substrate process was selected to provide a low inductance wiring environment for densely packed mixed-signal IC applications. Additionally, the thin dielectric improves thermal heat-sinking, and provides low inductance access to the backside ground plane. In the tuned amplifier design, it was found that these advantages were mitigated by the high resistive losses incurred in the transmission line matching networks. Simulation of the circuit with lossless matching networks resulted in a 2.0 dB increase in the gain. Given that resistive losses increase inversely with substrate thickness for a line of constant characteristic impedance, increasing the dielectric thickness may be beneficial for circuits utilizing transmission line matching networks. Another transmission line alternative that is being considered is the use of airbridge microstrip-line structures.

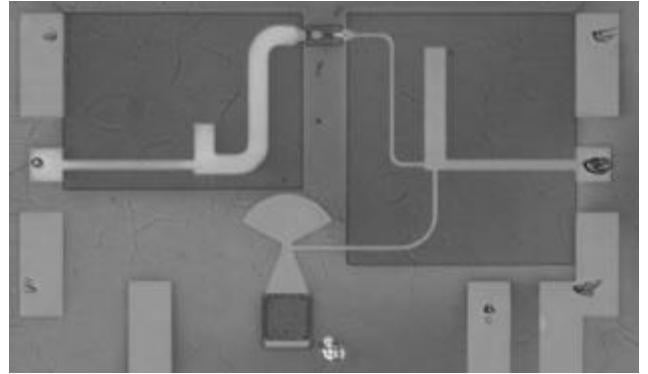


Fig. 5. Chip photograph of amplifier. Dimensions  $690 \mu\text{m} \times 350 \mu\text{m}$ .

### IV. RESULTS

The amplifier was measured on wafer from 140-220 GHz. The measurements were made using the HP8510C VNA with Oleson Microwave Labs Millimeter Wave VNA Extensions. The test set extensions are connected to GGB Industries coplanar wafer probes via a short length of WR-5 waveguide. The waveguide has enough flexibility to allow the probes sufficient range of motion ( $>2\text{mm}$ ) for on wafer testing. The measurements were calibrated using on wafer TRL standards.

Fig. 6 shows the measured gain of the amplifier. The bias conditions for the transistor were  $V_{CE} = 1.2 \text{ V}$ , and  $I_C = 2.4 \text{ mA}$ . A maximum gain of 3.0 dB was obtained at 185 GHz. The measured input and output return loss of the amplifier is shown in Fig. 7.

The gain of the amplifier was considerably less than the 6.5 dB peak predicted by simulation. However, measurements of individual devices on the wafer appear to show poorer RF performance than the device that the transistor model was based on. The input and output matches of the amplifier were both shifted downwards from the 200 GHz design frequency. At the time of this writing, the S-parameters of individual devices had not been extracted; therefore, it was not clear whether the mismatch was due to inaccuracies in modeling the active or passive circuit elements.

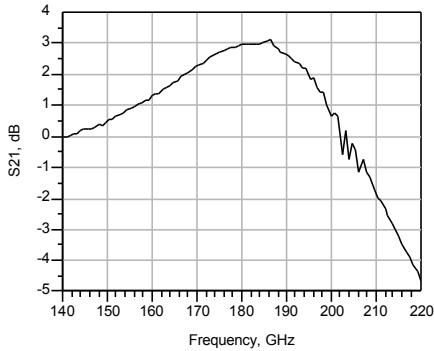


Fig. 6. Measured gain of single stage amplifier.

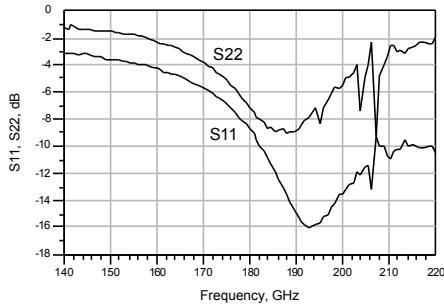


Fig. 7. Measured input and output return loss of amplifier.

## V. CONCLUSION

We have presented the first HBT tuned amplifier designed in the 140-220 GHz band. The single-stage amplifier exhibited a peak gain of 3.0 dB at 185 GHz. This simple circuit demonstrates the potential of the transferred-substrate technology for submillimeter wave monolithic IC applications.

## ACKNOWLEDGEMENT

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